Notice of Allowability	Application No.	Applicant(s)	
	10/708,608	IADANZA ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendments & Remarks filed 02/21/2006*.

2. ☒ The allowed claim(s) is/are *1-22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Applicants' attorney *Mohammad S. Rahman* gave authorization for this examiner's amendment on April 28, 2006. The application has been amended, based on Amendments filed on 02/21/2006, as follows:

Claim 1, line 1, change "circuits" to **—a custom circuit—**.

Claim 1, after line 3, insert —

schematically simulating said custom circuit;

back annotating to a schematic circuit which of said transistors use direct-fit models and which of said transistors are interpolated;—.

Claim 1, line 6, before "characterized" insert **—set of—**.
Claim 1, line 6, before "interpolated" insert **—set of—**.
Claim 1, line 7, change "circuits" to **—custom circuit—**.

Claim 2, line 2 – 4, delete **—schematically simulating a custom circuit... said transistors are interpolated;—**.

Claim 2, line 7, change "said" to **—the—**.
Claim 2, line 9, before "saturation" insert **—said—**.

Claim 5, line 1, before "interpolated" insert **—set of—**.
Claim 5, line 2, before "characterized" insert **—set of—**.

Claim 6, line 2, before "characterized" insert **—set of—**.
Claim 6, line 4, before "characterized" insert **—set of—**.
Claim 6, line 6, before "interpolated" insert **—set of—**.
Claim 6, line 7, before "characterized" insert **—set of—**.
Claim 6, line 8, before "characterized" insert **—set of—**.

Claim 8, line 1, change "electrical circuits" to **—a custom circuit—**.
Claim 8, line 2, delete **—a set of—**.
Claim 8, line 3, delete **—a set of—**.

Claim 8, after line 3, insert —

schematically simulating said custom circuit;

back annotating to a schematic circuit which of said devices use said direct-fit models and which of said devices are interpolated;—.

Claim 8, line 4, before "direct-fit" delete —**set of**—.

Claim 8, line 6, change "circuits" to —**custom circuit**—.

Claim 9, line 2 – 4, delete —**schematically simulating a custom circuit... said devices are interpolated;**—.

Claim 9, line 7, change "said" to —**the**—.

Claim 9, line 9, before "saturation" insert —**said**—.

Claim 14, line 3, change "transistor" to —**device**—.

Claim 15, line 1, before "computer" insert —**a**—.

Claim 15, line 3, change "circuits" to —**a custom circuit**—.

Claim 15, line 4, delete —**a set of**—.

Claim 15, line 5, delete —**a set of**—.

Claim 15, after line 5, insert —

schematically simulating said custom circuit;

back annotating to a schematic circuit which of said transistor devices use direct-fit models and which of said transistor devices are interpolated;—.

Claim 15, line 6, before "characterized" delete —**set of**—.

Claim 15, line 9, change "circuits" to —**custom circuit**—.

Claim 16, line 3 – 5, delete —**schematically simulating a custom circuit... said transistor devices are interpolated;**—.

Claim 16, line 8, change "said" to —**the**—.

Claim 16, line 10, before "saturation" insert —**said**—.

Claim 22, line 1, change "circuits" to —**a custom circuit**—.

Claim 22, line 2, delete —**a set of**—.

Claim 22, line 3, delete —**a set of**—.

Claim 22, after line 3, insert —

schematically simulating said custom circuit;

determining whether said transistors are in any of cutoff, saturation, static linear, and dynamic linear mode during simulation of said custom circuit;

extracting the saturation and dynamic linear mode transistors;—.

Claim 22, line 4, before "characterized" delete **—set of—**.

Claim 22, line 6, change "circuits" to **—custom circuit—**.

Claim 22, line 7, before "transistors" insert **—saturation and dynamic linear mode—**.

Reasons for Allowance

Claims 1 – 22 are allowed over the prior art of record. An examiner's statement of reasons for allowance is given in the following:

Claims 1 – 22 are allowed because the prior art does not teach or fairly suggest the following subject matter:

- A method of analyzing a custom circuit, said method comprising *back annotating to a schematic circuit which of transistors use direct-fit models and which of transistors are interpolated*, *analyzing said transistors within a netlist for matches in a set of characterized models created* and *providing a choice of using the matched set of characterized models or one of set of interpolated models created in designing said custom circuit* in combination with other limitation recited in independent **Claim 1**;
- A method of analyzing a custom circuit, said method comprising *back annotating to a schematic circuit which of devices use direct-fit models created and which of devices are interpolated*, *analyzing said devices within a netlist for matches in said direct-fit models* and *providing a choice of using the matched direct-fit models or one of interpolated models created in designing said custom circuit* in combination with other limitation recited in independent **Claim 8**;
- A program storage device readable by computer, tangibly embodying a program of instructions executable by said computer to perform a method of analyzing a custom circuit, said method comprising *back annotating to a*

schematic circuit which of transistor devices use direct-fit models and which of transistor devices are interpolated, *analyzing said transistor devices within a netlist for matches in a set of characterized models created* and *providing a choice of using the matched characterized models or one of interpolated models created in designing said custom circuit* in combination with other limitation recited in independent **Claim 15**;

- A method of analyzing a custom circuit, the method comprising *schematically simulation said custom circuit*, *extracting saturation and dynamic linear mode transistors in said customer circuit* and *performing sensitivity analysis on said saturation and dynamic linear mode transistors* in combination with other limitation recited in independent **Claim 22**.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272 – 1899. The examiner can normally be reached on Monday to Friday from 9:30am to 6:30pm.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun J. Lin
Primary Examiner
Art Unit 2825
April 28, 2006

SUN JAMES LIN
PRIMARY EXAMINER